



Intel® Desktop Board D815EEA2/D815EPEA2 Specification Update

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The desktop board D815EEA2/D815EPEA2 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are documented in this Specification Update.

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The Intel® desktop board D815EEA2/D815EPEA2 may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

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REVISION HISTORY

Date of Revision	Version	Description
April 2001	-001	This document is the first Specification Update for the Intel® Desktop Board D815EEA2/D815EPEA2.
May 2001	-002	Added Erratum 1.
June 2001	-003	Added Erratum 2. Revision –002 of the Technical Product Specification has been published. Please discard the earlier version.
August 2001	-004	Added Documentation Changes 1, 2.
September 2001	-005	Added erratum 3.
October 2001	-006	Added Erratum 4.
November 2001	-007	Added Specification Change 1. Updated Erratum 3.
January 2002	-008	Added Specification Clarifications 1, 2.
February 2002	-009	Added Erratum 5.

PREFACE

This document is an update to the specifications contained in the *Desktop Board D815EEA2/D815EPEA2 Technical Product Specification* (Order number A46399). It is intended for hardware system manufacturers and software developers of applications, operating systems, or tools. It will contain Specification Changes, Errata, Specification Clarifications, and Documentation Changes.

Refer to the *Pentium® III Processor Specification Update* (Order number 244453) for specification updates concerning the Pentium III processor. Items contained in the *Pentium III Processor Specification Update* that either do not apply to the desktop board D815EEA2/D815EPEA2 or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® Celeron® Processor Specification Update* (Order number 243748) for specification updates concerning the Intel Celeron processor. Items contained in the *Intel Celeron Processor Specification Update* that either do not apply to the desktop board D815EEA2/D815EPEA2 or have been worked around are noted in this document. Otherwise, it should be assumed that any processor errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82815 Chipset: 82815 Graphics and Memory Controller Hub (GMCH) Specification Update* (Order Number 290659) for specification updates concerning the 82815 GMCH Controller. Items contained in the *82815 GMCH Specification Update* that either do not apply to the desktop board D815EEA2/D815EPEA2 or have been worked around are noted in this document. Otherwise, it should be assumed that any GMCH errata for a given stepping are applicable to the PBA revision(s) associated with that stepping.

Refer to the *Intel® 82801 I/O Controller Hub (ICH) Specification Update* (Order Number 290677) for specification updates concerning the 82801 I/O Controller Hub. Items contained in the *Intel 82801 ICH Specification Update* that either do not apply to the desktop board D815EEA2/D815EPEA2 or have been worked around are noted in this document. Otherwise, it should be assumed that any ICH errata for a given stepping are applicable to the Printed Board Assembly (PBA) revision(s) associated with that stepping.

Nomenclature

Specification Changes are modifications to the current published specifications. These changes will be incorporated in the next release of the specifications.

Errata are design defects or errors. Characterized errata may cause the desktop board D815EEA2/D815EPEA2 behavior to deviate from published specifications. Hardware and software designed to be used with any given Printed Board Assembly (PBA) and BIOS revision level must assume that all errata documented for that PBA and BIOS revision level are present on all desktop boards.

Specification Clarifications describe a specification in greater detail or further highlight a specification's impact to a complex design situation. These clarifications will be incorporated in the next release of the specifications.

Documentation Changes include typos, errors, or omissions from the current published specifications. These changes will be incorporated in the next release of the specifications.

**Specification Update for
Desktop Board D815EEA2/D815EPEA2**

**GENERAL INFORMATION****Basic Desktop Board D815EEA2/D815EPEA2 Identification Information**

AA Revision	PBA Revision	BIOS Revision	Notes
A45154-204	A45155-204	EA81520A.86A.0006.P03	1-6
A45154-205	A45155-205	EA81520A.86A.0007.P04	1-6
A45154-206	A45155-206	EA81520A.86A.0007.P04	1-6
A45154-207	A45155-207	EA81520A.86A.0015.P10	1-6
A45154-208	A45155-208	EA81520A.86A.0021.P13	1-6
A45156-204	A45157-204	EA81520A.86A.0006.P03	1-6
A45156-205	A45157-205	EA81520A.86A.0006.P03	1-6
A45156-206	A45157-206	EA81520A.86A.0015.P10	1-6
A45156-207	A45157-207	EA81520A.86A.0021.P13	1-6
A54453-205	A54454-205	EA81520A.86A.0007.P04	1-6
A54453-206	A54454-206	EA81520A.86A.0007.P04	1-6
A54453-207	A54454-207	EA81520A.86A.0015.P10	1-6
A54453-208	A54454-208	EA81520A.86A.0021.P13	1-6
A52399-802	A52400-802	EA81520A.86A.0017.P11	1-6
A52399-803	A52400-803	EA81520A.86A.0028.P15	1-6
A52395-802	A52396-802	EA81520A.86A.0017.P11	1-6
A52395-803	A52396-803	EA81520A.86A.0028.P15	1-6
A55991-802	A55992-802	EA81520A.86A.0017.P11	1-6
A55991-803	A55992-803	EA81520A.86A.0028.P15	1-6

NOTES:

- The PBA number or AA number is found on a small label on the component side of the board.
- The 82815 Chipset kit used on this PBA revision consists of three components as follows:

Device	Stepping	S-Spec Numbers
82815 GMCH or	A2 B0 A2T	SL4DF SL5NQ SL5YN
82815EP MCH	A2 B0	SL552 SL5NR
82801BA ICH	B1 B0	SL4HM SL5FC



Device	Stepping	S-Spec Numbers
SST 49L004A33 FWH	NA	NA

3. The following errata are contained in the *Pentium® III Processor Specification Update* (Order Number 244453) for the Pentium III processor and either do not apply to the Desktop Board D815EEA2/D815EPEA2 or have been worked-around in this PBA and/or BIOS revision: 1. All other errata associated with the processor apply to this PBA revision.
4. The following errata are contained in the *Intel® Celeron® Processor Specification Update* (Order Number 243748) for the Celeron processor and either do not apply to the Desktop Board D815EEA2/D815EPEA2 or have been worked-around in this PBA and/or BIOS revision: None. All other errata associated with the processor apply to this PBA revision.
5. The following items are contained in the *Intel® 82815 Graphics and Memory Controller Hub (GMCH) Specification Update* (Order Number 290659) and either do not apply to the Desktop Board D815EEA2/D815EPEA2 or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the GMCH apply to this PBA revision.
6. The following items are contained in the *Intel® 82801 I/O Controller Hub Specification Update* (Order Number 290677) and either do not apply to the Desktop Board D815EEA2/D815EPEA2 or have been worked around in this PBA and/or BIOS revision: None. All other errata associated with the ICH apply to this PBA revision.

Summary Table of Changes

The following table indicates the Specification Changes, Errata, Specification Clarifications, or Documentation Changes which apply to the desktop board D815EEA2/D815EPEA2. Intel intends to fix some of the errata in a future revision of the desktop board, and to account for the other outstanding issues through documentation or specification changes as noted. This table uses the following notations:

CODES USED IN SUMMARY TABLE

- Doc: Document change or update that will be implemented.
- Fix: This erratum is intended to be fixed in a future revision of the desktop board or BIOS.
- Fixed: This erratum has been previously fixed.
- NoFix: There are no plans to fix this erratum.
- Shaded: This erratum is either new or modified from the previous version of the document.

NO.	PLANS	SPECIFICATION CHANGES
1	Doc	Support for faster Intel® Pentium® III processors
NO.	PLANS	ERRATA
1	Fixed	Intel Pentium III processor Erratum E76
2	Fix	System BIOS will not properly configure multi-channel audio Communications Network Riser (CNR) cards
3	Fixed	Communication Network Riser (CNR) LAN devices may not respond upon returning from S4 or S5 ACPI sleep states
4	Fixed	Advanced Power Management (APM) feature set to disabled in the BIOS Setup Menu will cause system reboot if the user attempts a system shutdown during POST
5	Fixed	System hang during POST may occur when using certain USB cameras
NO.	PLANS	SPECIFICATION CLARIFICATIONS
1	Doc	Change to description of Section 2.6, Interrupts
2	Doc	Change to description of Section 2.7, PCI Interrupt Routing Map
NO.	PLANS	DOCUMENTATION CHANGES
1	Doc	Change to description of Section 2.8.2.2, Figure 14, Audio, Video, Power, and Hardware Control Connectors
2	Doc	Change to description of Section 2.8.2.2, Table 37, Chassis Intrusion Connector

SPECIFICATION CHANGES

The Specification Changes listed in this section apply to the *D815EEA2/D815EPEA2 Desktop Board Technical Product Specification* (Order Number A46399). All Specification Changes will be incorporated into a future version of that specification.

1. Support For Faster Intel® Pentium® III Processors

Section 1.6, Processor, will change in its entirety as follows:

1.6 Processor



CAUTION

Use only the processors listed below. Use of unsupported processors can damage the board, the processor, and the power supply. See the Intel® Desktop D815EEA2/D815EPEA2 Specification Update for the most up-to-date list of supported processors for the D815EEA2 and D815EPEA2 boards.

The D815EEA2 and D815EPEA2 boards both support a single Pentium® III or Celeron® processor. The system bus frequency is automatically selected. The D815EEA2 and D815EPEA2 boards support the processors listed in Table 1.

Table 1. Supported Processors

Type	Designation	System Bus Frequency	L2 Cache Size
Pentium® III processor in an FC-PGA package	533EB, 600EB, 667, 733, 800EB, 866, and 933 MHz	133 MHz	256 KB
	1.0, and 1.2 GHz		
	500E, 550E, 600E, 650, 700, 750, 800, and 850, MHz	100 MHz	256 KB
	1.1 GHz		
Celeron® processor in an FC-PGA package	800, 850, 900 and 950 MHz	100 MHz	128 KB
	1.1 GHz		
	533A, 566, 600, 633, 667, 700, 733, and 766 MHz	66 MHz	128 KB

**NOTE**

BIOS revision EA81520A.86A.0028.P12 or greater and board revisions A52395-7xx, A52399-7xx, and A55991-7xx or greater are required for the board to properly support 1.2 GHz or later processors.

**NOTE**

BIOS revision EA81520A.86A.0019.P12 or greater is required for the board to properly support 900 MHz Celeron® or later processors.

All supported onboard memory can be cached, up to the cachability limit of the processor. See the processor's data sheet for cachability limits.

For information about	Refer to
Product information on supported processors	Section 1.3, page 19
Processor data sheets	Section 1.3, page 19

ERRATA

1. **Intel® Pentium® III Processor Erratum E76**

PROBLEM: For a complete description of the Pentium® III processor erratum E76, see the Pentium III Specification Update, order number 244453 found at <http://developer.intel.com/design/PentiumIII/specupdt/>.

IMPLICATION: For a complete description of the Pentium III processor erratum E76, see the Pentium III Specification Update, order number 244453 found at <http://developer.intel.com/design/PentiumIII/specupdt/>.

WORKAROUND: Update the D815EEA2/D815EPEA2 desktop board with BIOS revision EA81520A.86A.0014.P09.

STATUS: This erratum was addressed in BIOS revision EA81520A.86A.0014.P09.

2. **System BIOS Will Not Properly Configure Multi-Channel Audio Communications Network Riser (CNR) Cards**

PROBLEM: During the system boot process, the system BIOS compares the multi-channel signature stored in BIOS with the multi-channel signature stored in the audio CNR EEPROM. If the signatures match, the system BIOS then programs the device ID in the PCI configuration space with the multi-channel model ID from the CNR EEPROM. The system BIOS for this desktop board incorrectly programs the device ID in the PCI configuration space. When the audio driver that supports multi-channel functionality is installed, the driver may not install correctly or may not install at all.

IMPLICATION: Users who install a multi-channel audio CNR card may experience difficulty installing the manufacturers audio drivers.

WORKAROUND: None.

STATUS: This erratum is intended to be fixed in a future BIOS revision.

3. **Communication Network Riser (CNR) LAN Devices May Not Respond Upon Returning From S4 or S5 ACPI Sleep States**

PROBLEM: CNR LAN devices may not correctly resume from an S4 or S5 ACPI sleep state, even though the Microsoft Windows* operating system device manager indicates the device is working properly.

IMPLICATION: Users utilizing an add-in CNR LAN adapter with ACPI enabled may experience a loss of network connectivity after the system resumes from an ACPI S4 or S5 sleep state.

WORKAROUND: After resuming from the ACPI sleep state, the system will need to be restarted so that the CNR LAN device can be re-enumerated.

STATUS: This erratum was fixed in BIOS revision EA81520A.86A.0021.P13.

4. *Advanced Power Management (APM) Feature Set to Disabled in The BIOS Setup Menu Will Cause System Reboot if The User Attempts a System Shutdown During POST*

PROBLEM: If the APM function is set to disabled in the BIOS setup menu and the user attempts a system shutdown during POST, the system will reboot instead of shutting down.

IMPLICATION: Users who wish to perform a system shutdown during POST will experience a reboot and not a system shutdown as expected if the APM function is set to disabled in the BIOS setup menu.

WORKAROUND: None.

STATUS: This erratum was fixed in BIOS revision EA81520A.86A.0021.P13.

5. *System Hang During POST May Occur When Using Certain USB Cameras*

PROBLEM: During the system boot, certain USB cameras may cause a hang during POST if the camera is on during the boot process.

IMPLICATION: Some USB cameras may cause a system hang if the camera is on during system boot due to the BIOS incorrectly identifying the camera as a bootable device.

WORKAROUND: Ensure that the USB camera is off during the system boot process.

STATUS: This erratum was fixed in BIOS revision EA81520A.86A.0030.P16.

SPECIFICATION CLARIFICATIONS

The Specification Changes listed in this section apply to the *D815EEA2/D815EPEA2 Desktop Board Technical Product Specification* (Order Number A46399). All Specification Changes will be incorporated into a future version of that specification.

1. *Change to Description of Section 2.6, Interrupts*

Section 2.6, Interrupts, will change in its entirety as follows:

2.6 *Interrupts*

The Interrupts can go through either the Programmable Interrupt Controller (PIC) or the Advanced Programmable Interrupt Controller (APIC) portion of the Intel ICH2 component. The PIC is supported in Windows* 98 SE and Windows ME and uses the first 16 interrupts. The APIC is supported in Windows 2000 and Windows XP and support a total of 24 interrupts.

Table 17. Interrupts

IRQ	System Resource
NMI	I/O channel check
0	Reserved, interval timer
1	Reserved, keyboard buffer full
2	Reserved, cascade interrupt from slave PIC
3	COM2 (Note 1)
4	COM1 (Note 1)
5	LPT2 (Plug and Play option) / User available
6	Diskette drive
7	LPT1 (Note 1)
8	Real-time clock
9	Reserved for Intel ICH2 system management bus
10	User available
11	User available
12	Onboard mouse port (if present, else user available)
13	Reserved, math coprocessor
14	Primary IDE (if present, else user available)
15	Secondary IDE (if present, else user available)

continued

Table 17. Interrupts (continued)

IRQ	System Resource
16	AGP video (through PIRQA) ^(Note 2)
17	AC' 97 Audio/User Available (through PIRQB) ^(Note 2)
18	User available (through PIRQC) ^(Note 2)
19	Intel® ICH2 USB Controller #1 (through PIRQD) ^(Note 2)
20	Intel ICH2 LAN (optional) (through PIRQE) ^(Note 2)
21	User available (through PIRQF) ^(Note 2)
22	User available (through PIRQG) ^(Note 2)
23	Intel ICH2 USB Controller #2/ User Available (through PIRQH) ^(Note 2)

Note 1: Default, but can be changed to another IRQ.

Note 2: Available in APIC mode only.

2. *Change to Description of Section 2.7, PCI Interrupt Routing Map*

Section 2.7, PCI Interrupt Routing Map, will change in its entirety as follows:

2.7 *PCI Interrupt Routing Map*

This section describes interrupt sharing and how the interrupt signals are connected between the PCI bus connectors and onboard PCI devices. The PCI specification specifies how interrupts can be shared between devices attached to the PCI bus. In most cases, the small amount of latency added by interrupt sharing does not affect the operation or throughput of the devices. In some special cases where maximum performance is needed from a device, a PCI device should not share an interrupt with other PCI devices. Use the following information to avoid sharing an interrupt with a PCI add-in card.

PCI devices are categorized as follows to specify their interrupt grouping:

- **INTA:** By default, all add-in cards that require only one interrupt are in this category. For almost all cards that require more than one interrupt, the first interrupt on the card is also classified as INTA.
- **INTB:** Generally, the second interrupt on add-in cards that require two or more interrupts is classified as INTB. (This is not an absolute requirement.)
- **INTC and INTD:** Generally, a third interrupt on add-in cards is classified as INTC and a fourth interrupt is classified as INTD.

The Intel ICH2 has eight programmable interrupt request (PIRQ) input signals. All PCI interrupt sources either onboard or from a PCI add-in card connect to one of these PIRQ signals. Some PCI interrupt sources are electrically tied together on the D815EEA2 and D815EPEA2 boards and therefore share the same interrupt. Table 18 shows an example of how the PIRQ signals are routed on the D815EEA2 and D815EPEA2 boards.

For example, using Table 18 as a reference, assume that an add-in card using INTA is plugged into PCI bus connector 3. In PCI bus connector 3, INTA is connected to PIRQH, which is already connected to Intel ICH2 USB controller #2. The add-in card in PCI bus connector 3 now shares interrupts with these onboard interrupt sources.

Table 18. PCI Interrupt Routing Map

PCI Interrupt Source	ICH PIRQ Signal Name				
	PIRQF	PIRQG	PIRQH	PIRQB	Other
GMCH/AGP				INTB	INTA to PIRQA
Intel® ICH2 USB controller #1					INTD to PIRQD
SMBus controller				INTB	
Intel ICH2 USB controller #2			INTC		
Intel ICH2 audio/modem				INTB	
Intel ICH2 LAN					INTA to PIRQE
PCI bus connector 1 (J7B1)	INTA	INTB	INTC	INTD	
PCI bus connector 2 (J8B2)	INTD	INTA	INTB	INTC	
PCI bus connector 3 (J9B2)	INTC	INTD	INTA	INTB	
PCI bus connector 4 (J9B1)	INTB	INTC	INTD	INTA	
PCI bus connector 5 (J10B1)	INTA	INTB	INTC	INTD	

 **NOTE**

In PIC mode, the Intel ICH2 can connect each PIRQ line internally to one of the IRQ signals (3, 4, 5, 6, 7, 9, 10, 11, 12, 14, and 15). Typically, a device that does not share a PIRQ line will have a unique interrupt. However, in certain interrupt-constrained situations, it is possible for two or more of the PIRQ lines to be connected to the same IRQ signal. In APIC mode, the allocation of PIRQ lines to IRQ signals is as shown in Table 18.

DOCUMENTATION CHANGES

The Documentation Changes listed in this section apply to the *D815EEA2/D815EPEA2 Desktop Board Technical Product Specification* (Order Number A46399). All Documentation Changes will be incorporated into a future version of that specification.

1. **Change to Description of Section 2.8.2.2, Figure 14, Audio, Video, Power, and Hardware Control Connectors**

Section 2.8.2.2, Figure 14, audio, Video, Power, and Hardware Control Connectors will change in its entirety as follows:

Item	Description	Color	Reference Designator	For more information see:
A	Auxiliary line in, ATAPI style	White	J6B4	Table 29
B	Front panel audio (optional)	White	J6B2	Table 30
C	ATAPI CD-ROM	Black	J6B3	Table 31
D	Digital video out (optional)	N/A	J5C1	Table 32
E	Processor fan (fan 1)	N/A	J1B1	Table 33
F	Power	N/A	J4H1	Table 34
G	Chassis fan (fan 3) (optional)	N/A	J4G1	Table 35
H	System fan (fan 2)	N/A	J9H1	Table 36
I	Chassis intrusion (optional)	N/A	J9H4	Table 37
J	Wake on LAN* technology (optional)	N/A	J9G1	Table 38

Figure14. Audio, Video, Power, and Hardware Control Connectors

2. **Change to Description of Section 2.8.2.2, Table 37, Chassis Intrusion Connector**

Section 2.8.2.2, Table 37, Chassis Intrusion Connector, will be changed in its entirety as follows:

Table 37. Chassis Intrusion Connector (J9H4) (Optional)

Pin	Signal Name
1	INTRUDER#
2	Ground